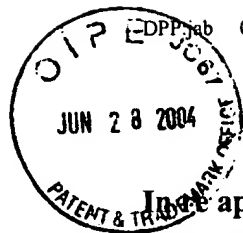


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06/23/04 1011-64535-01 288376.doc

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor application of: Bailey et al.

Application No. 09/883,838

Filed: June 17, 2001

Confirmation No. 9970

For: SYNCHRONIZATION OF MULTIPLE
SIMULATION DOMAINS IN AN EDA
SIMULATION ENVIRONMENT

Examiner:

Art Unit: 2123

Attorney Reference No. 1011-64535-01

CERTIFICATE OF MAILING

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Attorney
for Applicant(s)

Date Mailed June 23, 2004

**INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 C.F.R. § 1.97(b)(3)**

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Listed on the accompanying form PTO-1449 and enclosed herewith are several English-language and/or non-English-language documents. Applicants respectfully request that these documents be listed as references cited on the issued patent.

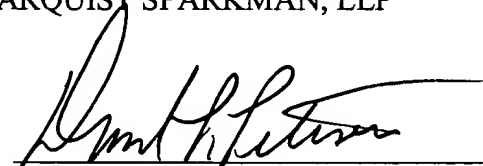
Applicants filed this Information Disclosure Statement ("IDS") before the mailing date of a first Office action on the merits. As a result, no fee should be required to file this IDS. However, if the Patent Office determines that a fee is required for Applicants to file this IDS, please charge any such fees, or credit overpayment, to Deposit Account No. 02-4550. A **duplicate** copy of this Information Disclosure Statement is enclosed.

The filing of this IDS shall not be construed to be an admission that the information cited in the statement is, or is considered to be, prior art or otherwise material to patentability as defined in 37 C.F.R. §1.56.

Respectfully submitted,

KLARQUIST SPARKMAN, LLP

By

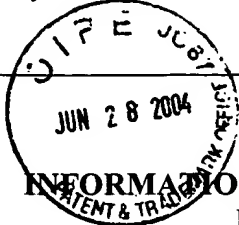


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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Attorney Docket Number	1011-64535-01
Application Number	09/883,838
Filing Date	June 17, 2001
First Named Inventor	Bailey et al.
Art Unit	2123
Examiner Name	

U.S. PATENT DOCUMENTS

NOTE: If this application was filed after June 30, 2003, copies of United States patents and United States published patent applications do not have to be provided to the Patent Office. This requirement of 37 C.F.R. § 1.98(a)(2)(i) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on August 5, 2003 (1276 OG 55).

Examiner's Initials*	Cite No. (optional)	Number	Publication Date	Name of Applicant or Patentee
		5,768,567	6/16/1998	Klein et al.

FOREIGN PATENT DOCUMENTS

Examiner's Initials*	Cite No. (optional)	Country	Number	Publication Date	Name of Applicant or Patentee
		EPA	0418980A2	9/20/1991	LSI Logic Corporation

OTHER DOCUMENTS

Examiner's Initials*	Cite No. (optional)	
		Yoo et al., "Fast Hardware-Software Coverification by Optimistic Execution of Real Processor", Proceedings Design, Automation and Test in Europe Conference and Exhibition 2000 (Cat. No. PR00537), Proceedings of Meeting on Design Automation and Test in Europe, Paris, France, 27-30 March 2000, pp. 663-668, XP002258737, 2000, Los Alamitos, CA, USA, IEEE Comput. Soc., USA.
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		Harris et al., "The Co-Verification of an RTOS in an SOC", Integrated System Design, May 2001, CMP Media, Inc., USA, Vol. 13, No. 143, pp. 23-30, XP008023502

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* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.